

MINIMUM HARDWARE IMPLEMENTATION OF MULTIPLIERS OF THE LIFTING WAVELET TRANSFORM

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ABSTRACT

The lifting structured wavelet transform (lifting wavelet) attracts researchers' attention as a key technology to a lossless and lossy unified coding system of digital image data. For VLSI circuit implementation, multiplier coefficients in the transform must be truncated into finite word length binary values. This report investigates how to appropriately assign error tolerance to each coefficient considering its sensitivity to a typical image signal under a given tolerable total hardware cost. As a result, it is confirmed that the total hardware scale of the multipliers is reduced to 51%.

1. INTRODUCTION

The lifting structured wavelet transform (lifting wavelet) attracts researchers' attention as a key technology to a lossless and lossy unified coding system of digital image data. The next international standard JPEG 2000 adopts this type of wavelet transform called 5/3 filter for "lossless" coding and 9/7 filter for "lossy" coding of images respectively [1, 2].

Multiplier coefficients of the 9/7 filter are initially given as real numbers. They are truncated into finite word length binary values for VLSI circuit implementation. No matter how the coefficients are truncated, almost no error due to finite word length expression is observed in the decoded signal as far as the same truncated coefficient set is shared between encoder and decoder in case of the lifting wavelet.

However, when it is supposed that various types of decoders are used to decode one bit stream, there still remains a problem what is the minimum word length to avoid encoder-decoder mismatching to maintain image quality of decoded signal. In case of DCT, a great deal of efforts has been made on evaluating minimum word length to avoid the mismatching according to H.261 [4]. On the contrary, what seems to be lacking is investigation on the lifting wavelet.

The purpose of this report is to explore a little further into finding minimum hardware implementation of multipliers in the decoder to avoid the encoder-decoder mismatching. Since word length does not always indicate hardware complexity of an LSI, an FPGA evaluation tool [5] is applied to our investigation and "Signed Power of Two (SPT)"

[6] structure is taken into account as an implementation style of the multipliers.

2. THE LIFTING WAVELET

2.1. Multiplier Coefficients

The lifting wavelet illustrated in figure 1 contains two tap linear phase FIR filters :

$$\begin{cases} H_0(z) = h_0(z+1) \\ H_1(z) = h_1(1+z^{-1}) \\ H_2(z) = h_2(z+1) \\ H_3(z) = h_3(1+z^{-1}) \end{cases} \quad (1)$$

Multiplier coefficient values of the 9/7 filter [1] to be truncated in this report are given by

$$\begin{cases} h_0 = -1.58613\ 43420\ 59924 \dots \\ h_1 = -0.05298\ 01185\ 72961 \dots \\ h_2 = 0.88291\ 10755\ 30934 \dots \\ h_3 = 0.44350\ 68520\ 43971 \dots \\ h_4 = 1.23017\ 41049\ 14001 \dots \\ h_5 = 1.62578\ 86132\ 23192 \dots \end{cases} \quad (2)$$

2.2. Transfer Function

Analysis part of the lifting wavelet in the encoder decomposes input signal $X(z)$ into two band signals $Y_L(z)$ and $Y_H(z)$.

$$\begin{bmatrix} Y_L(z) \\ Y_H(z) \end{bmatrix} = \mathbf{P}(z) \begin{bmatrix} \downarrow 2 & 0 \\ 0 & \downarrow 2 \end{bmatrix} \begin{bmatrix} 1 \\ z \end{bmatrix} X(z) \quad (3)$$

These signals are synthesized in the synthesis part of the transform in the decoder and the decoded signal $X'(z)$ is reconstructed.

$$X'(z) = \begin{bmatrix} 1 \\ z^{-1} \end{bmatrix}^T \begin{bmatrix} \uparrow 2 & 0 \\ 0 & \uparrow 2 \end{bmatrix} \mathbf{P}^{-1}(z) \begin{bmatrix} Y_L(z) \\ Y_H(z) \end{bmatrix} \quad (4)$$

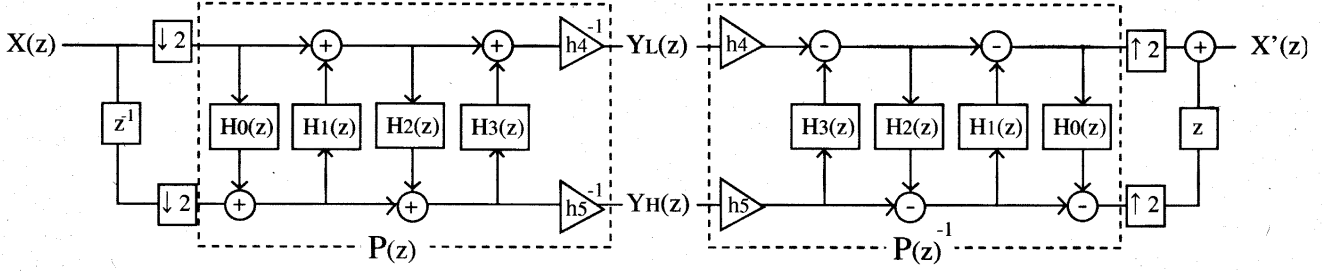


Fig. 1. Two channel lifting wavelet transform.

In the equations above, matrix $\mathbf{P}(z)$ is defined by

$$\mathbf{P}(z) = \mathbf{K} \cdot \mathbf{H}_3(z)\mathbf{H}_2(z)\mathbf{H}_1(z)\mathbf{H}_0(z) \quad (5)$$

$$\mathbf{H}_i(z) = \begin{bmatrix} 1 & 0 \\ H_i(z) & 1 \end{bmatrix} \quad i \text{ is even.} \quad (6)$$

$$\mathbf{H}_i(z) = \begin{bmatrix} 1 & H_i(z) \\ 0 & 1 \end{bmatrix} \quad i \text{ is odd.} \quad (7)$$

$$\mathbf{K} = \begin{bmatrix} h_4^{-1} & 0 \\ 0 & h_5^{-1} \end{bmatrix} \quad (8)$$

and

$$\begin{bmatrix} \downarrow 2 \cdot X(z) \\ \uparrow 2 \cdot X(z) \end{bmatrix} = \begin{bmatrix} \frac{1}{2} \sum_{p=0}^1 X(z^{1/2} e^{j\pi p}) \\ X(z^2) \end{bmatrix} \quad (9)$$

The two band splitting is repeated "N" times on the low band signal $Y_L(z)$ until there exists no correlation in the signal. It is called "N" stage decomposition.

3. COEFFICIENT SENSITIVITY

3.1. Error Signal in Decoded Signal

To investigate the encoder-decoder mismatching, similar to H.261 case for DCT [4], input signal $X(z)$ expressed with 8 bit integer value is embedded into forward lifting wavelet transform with almost infinite word length coefficients. Output signal is expressed with real numbers but rounded into integer to produce the signal $Y(z)$. In the decoding side, the backward wavelet transform is applied to the signal $Y(z)$ and its output signal is also rounded into integer to produce the signal $X'(z)$.

Defining the error signal $E(z)$ in the decoded signal $X'(z)$ as

$$E(z) = X'(z) - X(z) \quad (10)$$

it is expected to observe the error due to finite word length expression of only one coefficient h_i , $i \in 0, 1, \dots, 5$ in the decoder if and only if all the other coefficients are expressed with almost infinite word length. As a result of our calculations, the error signal $E(z)$ due to finite expression of h_i

where

$$\hat{h}_i = \Delta h_i + h_i \quad (11)$$

is summarized as follows for three stage decomposition for example.

i) Finite expression of h_i at the first stage.

$$E(z) = \Delta h_i \begin{bmatrix} \begin{bmatrix} G_L(z^4) \\ G_H(z^4)z^{-4} \end{bmatrix} G_L(z^2) \\ G_H(z^2)z^{-2} \\ \dot{G}_H(z)z^{-1} \end{bmatrix} \dot{G}_L(z) \end{bmatrix}^T \mathbf{M}_{44} \mathbf{Y}_{41} \quad (12)$$

ii) Finite expression of h_i at the second stage.

$$E(z) = \Delta h_i \begin{bmatrix} \begin{bmatrix} G_L(z^4) \\ G_H(z^4)z^{-4} \end{bmatrix} \dot{G}_L(z^2) \\ \dot{G}_H(z^2)z^{-2} \\ G_H(z)z^{-1} \end{bmatrix} G_L(z) \end{bmatrix}^T \mathbf{M}_{44} \mathbf{Y}_{41} \quad (13)$$

iii) Finite expression of h_i at the third stage.

$$E(z) = \Delta h_i \begin{bmatrix} \begin{bmatrix} \dot{G}_L(z^4) \\ \dot{G}_H(z^4)z^{-4} \end{bmatrix} G_L(z^2) \\ G_H(z^2)z^{-2} \\ G_H(z)z^{-1} \end{bmatrix} G_L(z) \end{bmatrix}^T \mathbf{M}_{44} \mathbf{Y}_{41} \quad (14)$$

where

$$\begin{bmatrix} G_L(z) \\ G_H(z) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & z^{-1} \end{bmatrix} \mathbf{P}^{-1}(z) \quad (15)$$

$$\begin{bmatrix} \dot{G}_L(z) \\ \dot{G}_H(z) \end{bmatrix} = \frac{\partial}{\partial h_i} \begin{bmatrix} G_L(z) \\ G_H(z) \end{bmatrix} \quad (16)$$

and

$$\mathbf{M}_{44} \mathbf{Y}_{41} = \begin{bmatrix} \uparrow 8 & 0 & 0 & 0 \\ 0 & \uparrow 8 & 0 & 0 \\ 0 & 0 & \uparrow 4 & 0 \\ 0 & 0 & 0 & \uparrow 2 \end{bmatrix} \begin{bmatrix} Y_{L3}(z) \\ Y_{H3}(z) \\ Y_{H2}(z) \\ Y_{H1}(z) \end{bmatrix} \quad (17)$$

Table 1. Coefficient sensitivity for AR(1) input signal.

stage	S_{h_0}	S_{h_1}	S_{h_2}	S_{h_3}	S_{h_4}	S_{h_5}
1	42.9	304.5	69.9	7.2	25.0	2.5
2	39.2	284.1	64.1	8.5	24.7	2.9
3	38.1	264.7	61.1	10.9	24.1	4.0

3.2. Coefficient Sensitivity [3]

Since each coefficient has different sensitivity to the error $E(z)$, it is preferable to assign smaller tolerance for Δh_i to relatively sensitive coefficient under a given allowable total error, equivalently, a given total circuit scale.

This report utilizes the SNR sensitivity [3] defined by

$$S_{h_i} \equiv \frac{\sigma_{E_i}}{\Delta h_i} \quad (18)$$

where

$$\sigma_{E_i}^2 = \mathcal{E} \left[\frac{1}{2\pi} \int_{-\pi}^{\pi} |E(e^{j\omega})|^2 d\omega \right] \quad (19)$$

and $\mathcal{E}[\cdot]$ denotes ensemble average. As a result, variance of the error signal $\sigma_{E_i}^2$ is calculated by substituting equations (12), (13), (14) into equation (19).

Numerical results are summarized in table 1 for 6 coefficients at each stage \times 3 stages = 18 coefficients. Input signal is an AR(1) model with $\rho = 0.95$ generated by

$$X(z) = \frac{W(z)}{1 - \rho z^{-1}} \quad (20)$$

where $W(z)$ is a white signal and $N = 2^{16}$ with $\max=127$ and $\min=-128$. It is observed that the sensitivity of each coefficient is approximately same at different stages. h_1 is the most sensitive and h_5 is the least.

4. IMPLEMENTATION OF THE COEFFICIENTS

In this section, we drive multiplier coefficients of the lifting structured wavelet transform to avoid the encoder-decoder mismatching under the minimum circuit scale utilizing the sensitivity table listed in table 1.

4.1. SPT Implementation

The signed power of two (SPT) implementation has been reported as one of useful ways for reduction of hardware scale of multipliers [6]. In this case, coefficient values in equation (2) are truncated into the SPT expression

$$\hat{h}_i = \sum_{k=1}^{T_i} B_i^{(k)} 2^{q_i^{(k)}} \quad (21)$$

Table 2. SPT parameter T is determined by error tolerance Δh_i for each coefficient.

T	Δh_0	Δh_1	Δh_2	Δh_3	Δh_4	Δh_5
1	0.4139	0.0095	0.1171	0.0565	0.2302	0.3742
2	0.0861	0.0017	0.0079	0.0060	0.0198	0.1258
3	0.0236	0.0002	0.0001	0.0018	0.0042	0.0008
4	0.0076	0.0000	0.0000	0.0001	0.0003	0.0002
\vdots	\vdots	\vdots	\vdots	\vdots	\vdots	\vdots

Table 3. Coefficient value \hat{h}_1 for implementation is determined by SPT parameter T .

T	\hat{h}_1
1	-2^{+1}
2	$-2^{+0} - 2^{-1}$
3	$-2^{+0} - 2^{-1} - 2^{-4}$
4	$-2^{+0} - 2^{-1} - 2^{-3} + 2^{-5}$
5	$-2^{+0} - 2^{-1} - 2^{-3} + 2^{-5} + 2^{-7}$
\vdots	\vdots

where $B^{(k)} \in \{-1, 1\}$, T and $q^{(k)}$ denote the number of terms and an arbitrary integer number. When a error tolerance \hat{h}_i is given, the number of terms T is determined by table 2, and then the truncated coefficient value for implementation is finally determined by equation (21) and table 3.

So far, it has been general to set the same T for each coefficient. However, this report is assigning different T for each coefficient considering its sensitivity to the error in the decoded signal and colored spectrum of the input signal.

4.2. Error Tolerance Assignment

We calculated the tolerable error for each coefficient as below. Firstly, it is considered that transformed signals are rounded into integers after wavelet transform since they are stored in integer frame memory and entropy coded. The error due to this rounding operation with variance σ_R^2 propagates trough backward wavelet transform and observed in the decoded signal with variance $\sigma_{E_R}^2$. Namely,

$$\sigma_{E_R}^2 = \sum_s \sigma_R^2 W_s \|G_s\|^2 \quad (22)$$

$$\sigma_R^2 = \frac{1}{12} \quad (23)$$

where s means frequency band of the wavelet and W_s is a weighting value due to the number of samples at each frequency band. $\|G_s\|^2$ denotes square norm of the backward wavelet transform.

Table 4. Coefficients for hardware implementation.

h_i	Proposed	Existing
h_0	$-2^{+0} - 2^{-1} - 2^{-3} + 2^{-5} + 2^{-7}$	$-2^{+0} - 2^{-1} - 2^{-3} + 2^{-5} + 2^{-7}$
h_1	$-2^{-4} - 2^{-12} + 2^{-7} + 2^{-9}$	$-2^{-4} - 2^{-7} - 2^{-12} + 2^{-6} + 2^{-9}$
h_2	$2^{+0} + 2^{-7} - 2^{-3}$	$2^{+0} + 2^{-7} + 2^{-13} - 2^{-3} - 2^{-15}$
h_3	$2^{-1} - 2^{-4}$	$2^{-1} + 2^{-7} + 2^{-13} - 2^{-4} - 2^{-9}$
h_4	$2^{+0} + 2^{-2} - 2^{-6} - 2^{-8}$	$2^{+0} + 2^{-2} - 2^{-6} - 2^{-8} - 2^{-12}$
h_5	$2^{+0} + 2^{-1} + 2^{-3}$	$2^{+0} + 2^{-1} + 2^{-3} + 2^{-10} - 2^{-12}$

On the other hand, the error due to the SPT (or finite word length) expression is in the decoded signal with variance $\sigma_{E_Q}^2$. Namely,

$$\sigma_{E_Q}^2 = \sum_i (S_{h_i} \cdot \Delta h_i)^2 \quad (24)$$

In this report, we determined the error tolerance Δh_i so that the following equation is satisfied.

$$10 \log_{10} \frac{255^2}{\sigma_{E_R}^2 + \sigma_{E_Q}^2} = 10 \log_{10} \frac{255^2}{\sigma_{E_R}^2} - \epsilon \quad (25)$$

4.3. Results of the Assignment

Table 4 lists up the result of our assignment. Three-stage wavelet decomposition is applied to AR(1) model with $\rho = 0.95$. ϵ is set to 0.25 [dB] and minimum value of the SPT is set to 2^{-16} . The SPT term T varies in the proposed method. Using this coefficient set, the encoder-decoder mismatching can be avoided.

We also compared hardware complexity of the coefficient set in the table with Verilog-HDL (FPGA Compiler ii 3.8) [5]. Results are illustrated in figure 2. As a result, circuit scale is reduced from 8186 [cell] to 4052 [cell]. This is 51% reduction of hardware scale.

5. SUMMARY

In this report, we proposed a new method for finding minimum hardware implementation of multipliers in the decoder to avoid the encoder-decoder mismatching. As a result, circuit scale was reduced from 8186 [cell] to 4052 [cell]. This was 51% reduction of hardware scale.

6. REFERENCES

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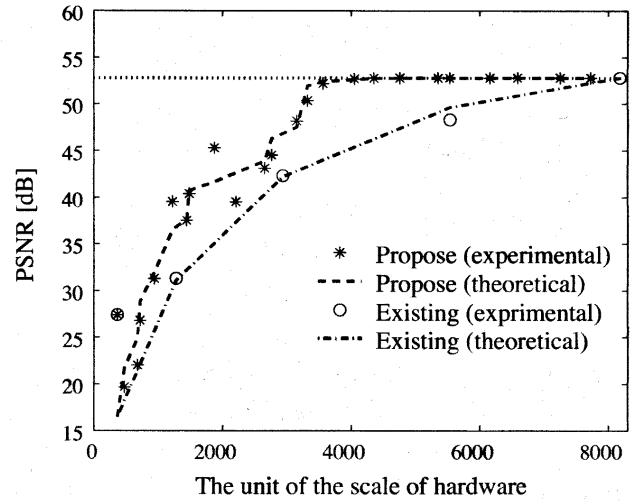


Fig. 2. Hardware complexity versus PSNR.

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